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EXAMINER	
GANDHI, DIPAKKUMAR B	

ART UNIT	PAPER NUMBER
2133	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/037,361	BYRD, JAMES M.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/11/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. The later-filed application must be an application for a patent for an invention which is also disclosed in the prior application (the parent or original nonprovisional application or provisional application); the disclosure of the invention in the parent application and in the later-filed application must be sufficient to comply with the requirements of the first paragraph of 35 U.S.C. 112. See *Transco Products, Inc. v. Performance Contracting, Inc.*, 38 F.3d 551, 32 USPQ2d 1077 (Fed. Cir. 1994).

2. An application in which the benefits of an earlier application are desired must contain a specific reference to the prior application(s) in the first sentence of the specification or in an application data sheet (37 CFR 1.78(a)(2) and (a)(5)). The specific reference to any prior nonprovisional application must include the relationship (i.e., continuation, divisional, or continuation-in-part) between the applications except when the reference is to a prior application of a CPA assigned the same application number.

Drawings

3. The drawings are objected to because

- In figure 6B, "Syndrome 18" is incorrect. It should be –Syndrome 16--.
- In figure 8A, "Error Detection/Correction Unit 306" is incorrect. It should be –Error Detection/Correction Unit 306A--.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of

any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities:

- On page 9, line 13, "receiver 1003" is incorrect. It should be —receiver 1002--.
- On page 9, line 14, "transmitter 902" is incorrect. It should be –transmitter 1001--.
- On page 9, line 15, "decoder 907" is incorrect. It should be –decoder 300--.
- On page 9, line 17, "decoder 907" is incorrect. It should be –decoder 300--.
- On page 13, line 23, "a0 XOR a1 XOR a2" is incorrect. It should be -- d0 XOR d1 XOR d2--.
- On page 15, line 18, "table 30A" is incorrect. It should be –table 40A--.
- On page 15, line 20, "table 30A" is incorrect. It should be –table 40A--.
- On page 15, line 24, 'check bit 12' is incorrect. It should be –check bit 14--.
- On page 16, line 11, "FIGs. 1D AND 1E" is incorrect. It should be –FIGs. 4D AND 4E--.
- On page 20, line 8, "Tester 300" is incorrect. It should be –Tester 200--.
- On page 20, line 12, "FIGs. 6C and 6D" is incorrect. It should be –FIG 6C-, as there is no figure 6D.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3-5, 24, 25, 27-29, 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurihara (US 4,107,649).

Kurihara anticipates claim 1.

Kurihara teaches a method of testing error correction/detection logic, the method comprising: creating an initial data bit combination having n bits, wherein each data bit in the initial data bit combination has a same logical value as each other data bit in the initial data bit combination; shifting a first bit having an different logical value than the same logical value across the initial data bit combination, wherein each time the first bit is shifted, one of n data bit combinations is generated; providing each of the n data bit combinations to the error detection/correction logic; in response to said providing, the error detection/correction logic generating a set of check bits for each of the n data bit combinations; comparing the set of check bits generated by the error correction/detection logic with a known correct set of check bits for each of the n data bit combinations; and dependent on an outcome of said comparing, generating an indication of whether the error detection/correction logic correctly generated the set of check bits (figure 2, col. 1, lines 44-60, col. 2, lines 12-19, Kurihara).

- Kurihara anticipates claim 3.

Kurihara teaches the method, further comprising: providing a set of m+1 test code words to the error correction/detection logic, wherein each code word has m bits, wherein a first test code word in the set of m+1 test code words is a correct code word, wherein each test code word other than the first test code word comprises a single-bit error at a different bit position within the code word than each other test code word; in response to said providing, the error correction/detection logic decoding the set of m+1 test code words; and verifying that the error correction/detection logic correctly decoded each of the m+1 test code words (figure 2, col. 2, lines 61-68, col. 3, lines 13-34, Kurihara).

- Kurihara anticipates claim 4.

Kurihara teaches the method wherein each bit in the first test code word has a same logical value, and wherein each test code word other than the first test code word comprises a bit having an opposite logical value at the different bit position (figure 2, col. 2, lines 61-62, col. 3, lines 39-47, lines 66-68, Kurihara).

- Kurihara anticipates claim 5.

Kurihara teaches the method, wherein providing a set of m+1 test code words comprises shifting the bit having the opposite logical value across the first test code word, wherein each time the bit is shifted, one

of the test code words other than the first test code word is created (figure 2, col. 3, lines 13-15, lines 66-68, Kurihara).

- Kurihara anticipates claim 24.

Kurihara teaches a tester for testing error correction/detection logic, the tester comprising: test check bit generating means for creating a set of test data bit combinations and providing the set of test data bit combinations to a check bit generator comprised in the error correction/detection logic, wherein the set of test data bit combinations comprises n n-bit data bit combinations, wherein each possible logical value of each data bit is present in at least one of the n n-bit data bit combinations in the set of test data bit combinations; comparison means for comparing check bits output by the error correction/detection logic for each of the n n-bit data bit combinations in the set of test data bit combinations to known correct check bits for each of the n n-bit data bit combinations; and indication means for generating an indication as to whether the check bits output by the error correction/detection logic are correct based on an output of the comparison means (figure 2, col. 5, lines 7-34, Kurihara).

- Kurihara anticipates claim 25.

Kurihara teaches test code word generating means for creating a set of test code words and providing the set of test code words to the error correction/detection logic, wherein the set of test code words comprises m+1 m-bit test code words, wherein a first test code word is a correct code word, and wherein each other test code word comprises a single-bit error, and wherein each of the other test code words comprises the single-bit error at a different bit position than any other of the other test code words; wherein the comparison means are further for comparing an output of the error correction/detection logic with a known correct output for each test code word in the set of test code words (figure 2, col. 2, lines 61-68, col. 3, lines 13-34, Kurihara).

- Kurihara anticipates claim 27.

Kurihara teaches a method of testing error correction/detection logic, the method comprising: providing a set of m+1 test code words to the error correction/detection logic, wherein each code word has m bits, wherein a first test code word in the set of m+1 test code words is a correct code word, wherein each test code word other than the first test code word comprises a single-bit error at a different bit position within

the code word than each other test code word; in response to said providing, the error correction/detection logic decoding the set of m+1 test code words; and verifying that the error correction/detection logic correctly decoded each of the m+1 test code words (figure 2, col. 2, lines 61-68, col. 3, lines 13-34, Kurihara).

- Kurihara anticipates claim 28.

Kurihara teaches the method, wherein each bit in the first test code word has a same logical value, and wherein each test code word other than the first test code word comprises a bit having an opposite logical value at the different bit position (figure 2, col. 2, lines 61-62, col. 3, lines 39-47, lines 66-68, Kurihara).

- Kurihara anticipates claim 29.

Kurihara teaches the method, wherein said providing comprises shifting the bit having the opposite logical value across the first test code word, wherein each time the bit is shifted, one of the test code words other than the first test code word is created (figure 2, col. 3, lines 13-15, lines 66-68, Kurihara).

- Kurihara anticipates claim 34.

Kurihara teaches a data processing system comprising: a storage array comprising at least one storage device; a host computer system coupled to provide data to the storage array; and error correction/detection logic configured to generate check bits for the data being provided to the storage array; wherein the host computer system is configured to test the error correction/detection logic by providing each of a set of n data bit combinations to the error detection/correction logic, wherein each data bit combination has n bits, wherein each possible value of each data bit is present in at least one of the n data bit combinations, wherein the set of n data bit combinations provided to the error detection/correction logic is a subset of a set of all data bit combinations that it is possible to create using n bits; wherein in response to being provided with the set of n data bit combinations, the error detection/correction logic is configured to generate a set of check bits for each of the n data bit combinations; and wherein the host computer system is configured to compare the set of check bits generated by the error correction/detection logic with a known correct set of check bits for each of the n data bit combinations (col. 3, lines 13-24, col. 5, line 52 - col. 6, line 14, Kurihara).

7. Claim 30 is rejected under 35 U.S.C. 102(b) as being anticipated by Arroyo et al. (US 5,502,732).

Arroyo et al. anticipate claim 30.

Arroyo et al. teach a method of testing error correction/detection logic, the method comprising: providing a set of test code words to the error correction/detection logic, wherein said providing comprises introducing an error into each of the test code words in the set by substituting check bits corresponding to an unused syndrome for a correct set of check bits within each test code word, wherein each test code word comprises substituted check bits corresponding to a different unused syndrome than each other test code word in the set of test code words; in response to said providing, the error correction/detection logic decoding each test code word in the set of test code words; and verifying that the error correction/detection logic correctly identified the error in each of the test code words (col. 5, line 55-col. 6, line 4, Arroyo et al.).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara (US 4,107,649) in view of Nielson et al. (US 5,619,642).

As per claim 2, Kurihara substantially teach the claimed invention described in claim 1 (as rejected above).

However Kurihara does not explicitly teach the specific use of the error detection/correction logic

comprising a Hamming code encoder and a Hamming code decoder.

Nielson et al. in an analogous art teach that another enhancement is the use of an EDC encoder and decoder, such as a Hamming code encoder and decoder, with the main RAM 60 (of FIG. 1), (col. 12, lines 28-30, Nielson et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kurihara's patent with the teachings of Nielson et al. by including an additional step of using the error detection/correction logic comprising a Hamming code encoder and a Hamming code decoder.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the error detection/correction logic comprising a Hamming code encoder and a Hamming code decoder would provide the opportunity to find the position of the error and correct the error by comparing the syndrome with the parity-check matrix H^T.

11. Claims 6-12, 26, 31-33, 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara (US 4,107,649) as applied to claim 3 above, and further in view of Arroyo et al. (US 5,502,732).

As per claim 6, Kurihara substantially teach the claimed invention described in claim 3 (as rejected above).

However Kurihara does not explicitly teach the specific use of verifying that the error correction/detection logic correctly decoded each of the m+1 test code words comprises verifying that the error correction/detection logic detects each of the single-bit errors.

Arroyo et al. in an analogous art teach that the present invention allows the test logic contained in a computer system to be tested during POST such that any errors can be determined and made available to the system software prior to beginning processing operations. Broadly, the present invention induces single and double bit errors, which the ECC logic must identify and correct, if possible. The CPU compares the data that is written to memory with the data that is read back. For single bit errors, the data should be identical since the ECC logic will identify and correct errors (col. 2, lines 10-20, Arroyo et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kurihara's patent with the teachings of Arroyo et al. by including an additional step of verifying that the error correction/detection logic correctly decoded each of the m+1 test code words comprises verifying that the error correction/detection logic detects each of the single-bit errors. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to determine if a single bit error is present in the code word and correct the error to provide error free data to the receiving system.

- As per claim 7, Kurihara and Arroyo et al. teach the additional limitations.

Arroyo et al. teach the method, wherein verifying that the error correction/detection logic correctly decoded each of the m+1 test code words comprises verifying that the error correction/detection logic corrects each of the single-bit errors that occurs in a data bit within each of the m+1 test code words (col. 2, lines 29-33, Arroyo et al.).

- As per claim 8, Kurihara and Arroyo et al. teach the additional limitations.

Arroyo et al. teach the method, wherein verifying that the error correction/detection logic correctly decoded each of the m+1 test code words comprises verifying that the error correction/detection logic indicates that the first test code word is correct in response to being provided with the first test code word (col. 8, lines 19-41, Arroyo et al.).

- As per claim 9, Kurihara and Arroyo et al. teach the additional limitations.

Arroyo et al. teach the method, further comprising: providing a set of test code words to the error correction/detection logic, wherein an error has been introduced into each of the test code words in the set by substituting check bits corresponding to an unused syndrome for a correct set of check bits within each test code word, wherein each test code word comprises substituted check bits corresponding to a different unused syndrome than each other test code word in the set of test code words; in response to said providing, the error correction/detection logic decoding each test code word in the set of test code words; and verifying that the error correction/detection logic correctly identified the error in each of the test code words (col. 5, line 55-col. 6, line 4, Arroyo et al.).

- As per claim 10, Kurihara and Arroyo et al. teach the additional limitations.

Kurihara teaches the method, wherein said providing a set of test code words comprises creating an initial code word, wherein each bit in the initial code word has a same logical value (figure 2, col. 3, lines 42-43, lines 66-68, Kurihara).

- As per claim 11, Kurihara and Arroyo et al. teach the additional limitations.

Kurihara teaches the method wherein the same logical value is a logical 0 (figure 2, col. 3, lines 42-43, lines 66-68, Kurihara).

Arroyo et al. teach that the substituted check bits in each code word equal a set of bits in one of the unused syndromes (col. 10, lines 31-33, Arroyo et al.).

- As per claim 12, Kurihara and Arroyo et al. teach the additional limitations.

Arroyo et al. teach the method, wherein the same logical value is a logical 1, and wherein each bit in the substituted check bits in each code word equals an inverse logical value of each bit in one of the unused syndromes (col. 9, line 50-col. 10, line 3, Arroyo et al.).

- As per claim 26, Kurihara and Arroyo et al. teach the additional limitations.

Arroyo et al. teach test code word generating means for creating a set of test code words and providing the set of test code words to the error correction/detection logic, wherein an error has been introduced into each of the test code words in the set by substituting check bits corresponding to an unused syndrome for a correct set of check bits within each test code word, wherein each test code word comprises substituted check bits corresponding to a different unused syndrome than each other test code word in the set of test code words; wherein the comparison means are further for comparing an output of the error correction/detection logic to a known correct output for each of the test code words (col. 5, line 55-col. 6, line 4, Arroyo et al.).

- As per claim 31, Kurihara and Arroyo et al. teach the additional limitations.

Kurihara teaches the method, wherein said providing comprises creating an initial code word, wherein each bit in the initial code word has a same logical value (figure 2, col. 3, lines 42-43, lines 66-68, Kurihara).

- As per claim 32, Kurihara and Arroyo et al. teach the additional limitations.

Kurihara teaches the method, wherein the same logical value is a logical 0 (figure 2, col. 3, lines 42-43, lines 66-68, Kurihara).

Arroyo et al. teach that the substituted check bits in each code word equal a set of bits in one of the unused syndromes (col. 10, lines 31-33, Arroyo et al.).

- As per claim 33, Kurihara and Arroyo et al. teach the additional limitations.

Arroyo et al. teach the method of claim 31, wherein the same logical value is a logical 1, and wherein each bit in the substituted check bits in each code word equals an inverse logical value of each bit in one of the unused syndromes (col. 9, line 50-col. 10, line 3, Arroyo et al.).

- As per claim 35, Kurihara and Arroyo et al. teach the additional limitations.

Kurihara teaches a method of testing error detection/correction logic, the method comprising: providing a subset of possible data bit combinations of n data bits to the error detection/correction logic, wherein the subset comprises n data bit combinations, wherein each possible value of each data bit is present in at least one of the n data bit combinations in the subset; verifying the error detection/correction logic by comparing a set of check bits generated by the error detection/correction logic for each of the n data bit combinations in the subset with a set of known correct check bits (figure 2, col. 1, lines 44-60, col. 2, lines 12-19, Kurihara).

Kurihara teaches providing a first set of m+1 test code words to the error detection/correction logic, wherein a first test code word is a correct test code word and where each other test code word in the set of m+1 test code words comprises a single-bit error, wherein each test code word having a single-bit error has the single-bit error at a different bit position than each other test code word that has a single-bit error; wherein said verifying further comprises comparing a first output of the error detection/correction logic generated in response to said providing a first set of m+1 test code words with a first known correct output for each of the m+1 test code words (figure 2, col. 2, lines 61-68, col. 3, lines 13-34, Kurihara).

Arroyo et al. teach providing a second set of test code words to the error detection/correction logic, wherein each test code word in the second set comprises an error introduced by substituting check bits corresponding to an unused syndrome for a correct set of check bits within a correct code word, wherein each test code word in the second set comprises substituted check bits corresponding to a different

unused syndrome than each other test code word in the second set of test code words; wherein said verifying further comprises comparing a second output of the error detection/correction logic generated in response to said providing a second set of test code words with a second known correct output for each of the m+1 test code words; and in response to said verifying, indicating whether the error detection/correction logic is operating properly (col. 5, line 55-col. 6, line 4, Arroyo et al.).

12. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara (US 4,107,649) in view of Fielder et al. (US 6,446,037 B1).

As per claim 13, Kurihara teaches to create an initial data bit combination having n bits, wherein each data bit in the initial data bit combination has a same logical value as each other data bit in the initial data bit combination; shift a first bit having an different logical value than the same logical value across the initial data bit combination, wherein each time the first bit is shifted, one of n data bit combinations is generated; provide each of the n data bit combinations to error detection/correction logic; compare a set of check bits generated by the error correction/detection logic with a known correct set of check bits for each of the n data bit combinations; and dependent on an outcome of said comparing, generate an indication of whether the error detection/correction logic correctly generated the set of check bits (figure 2, col. 1, lines 44-60, col. 2, lines 12-19, Kurihara).

However Kurihara does not explicitly teach the specific use of a computer readable medium comprising program instructions that are computer-executable.

Fielder et al. in an analogous art teach a program of instructions executable by a machine, such as a programmable digital signal processor or computer processor, to perform such a process can be conveyed by a medium readable by the machine, and the machine can read the medium to obtain the program and responsive thereto perform such process (col. 4, lines 60-64, Fielder et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kurihara's patent with the teachings of Fielder et al. by including an additional step of using a computer readable medium comprising program instructions that are computer-executable.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a computer readable

medium comprising program instructions that are computer-executable would provide the opportunity to perform the process fast and accurately.

- As per claim 14, Kurihara and Fielder et al. teach the additional limitations.

Kurihara teaches to provide a set of m+1 test code words to the error correction/detection logic, wherein each code word has m bits, wherein a first test code word in the set of m+1 test code words is a correct code word, wherein each test code word other than the first test code word comprises a single-bit error at a different bit position within the code word than each other test code word; and verify that the error correction/detection logic correctly decoded each of the m+1 test code words (figure 2, col. 2, lines 61-68, col. 3, lines 13-34, Kurihara). Fielder et al. teaches the computer readable medium comprising program instructions that are computer-executable (col. 4, lines 60-64, Fielder et al.).

- As per claim 15, Kurihara and Fielder et al. teach the additional limitations.

Kurihara teaches that each bit in the first test code word has a same logical value, and wherein each test code word other than the first test code word comprises a bit having an opposite logical value at the different bit position (figure 2, col. 2, lines 61-62, col. 3, lines 39-47, lines 66-68, Kurihara).

- As per claim 16, Kurihara and Fielder et al. teach the additional limitations.

Kurihara teaches to shift the bit having the opposite logical value across the first test code word, wherein each time the bit is shifted, one of the test code words other than the first test code word is created (figure 2, col. 3, lines 13-15, lines 66-68, Kurihara).

13. Claims 17-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara (US 4,107,649) and Fielder et al. (US 6,446,037 B1) as applied to claim 14 above, and further in view of Arroyo et al. (US 5,502,732).

As per claim 17, Kurihara and Fielder et al. substantially teach the claimed invention described in claim 14 (as rejected above).

However Kurihara and Fielder et al. do not explicitly teach the specific use of verifying that the error correction/detection logic detects each of the single-bit errors.

Arroyo et al. in an analogous art teach that the present invention allows the test logic contained in a computer system to be tested during POST such that any errors can be determined and made available

to the system software prior to beginning processing operations. Broadly, the present invention induces single and double bit errors, which the ECC logic must identify and correct, if possible. The CPU compares the data that is written to memory with the data that is read back. For single bit errors, the data should be identical since the ECC logic will identify and correct errors (col. 2, lines 10-20, Arroyo et al.). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kurihara's patent with the teachings of Arroyo et al. by including an additional step of verifying that the error correction/detection logic detects each of the single-bit errors.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that verifying that the error correction/detection logic detects each of the single-bit errors would provide the opportunity to determine if a single bit error is present in the code word and correct the error to provide error free data to the receiving system.

- As per claim 18, Kurihara, Fielder et al. and Arroyo et al. teach the additional limitations.

Arroyo et al. teach to verify that the error correction/detection logic corrects each of the single-bit errors that occur in a data bit within each of the m+1 test code words (col. 2, lines 29-33, Arroyo et al.).

- As per claim 19, Kurihara, Fielder et al. and Arroyo et al. teach the additional limitations.

Arroyo et al. teach to verify that the error correction/detection logic indicates that the first test code word is correct in response to being provided with the first test code word (col. 8, lines 19-41, Arroyo et al.).

- As per claim 20, Kurihara, Fielder et al. and Arroyo et al. teach the additional limitations.

Arroyo et al. teach to provide a set of test code words to the error correction/detection logic, wherein an error has been introduced into each of the test code words in the set by substituting check bits corresponding to an unused syndrome for a correct set of check bits within each test code word, wherein each test code word comprises substituted check bits corresponding to a different unused syndrome than each other test code word in the set of test code words; and verify that the error correction/detection logic correctly identified the error in each of the test code words (col. 5, line 55-col. 6, line 4, Arroyo et al.).

- As per claim 21, Kurihara, Fielder et al. and Arroyo et al. teach the additional limitations.

Kurihara teaches to create an initial code word, wherein each bit in the initial code word has a same logical value (figure 2, col. 3, lines 42-43, lines 66-68, Kurihara).

- As per claim 22, Kurihara, Fielder et al. and Arroyo et al. teach the additional limitations.

Kurihara teaches that the same logical value is a logical 0 (figure 2, col. 3, lines 42-43, lines 66-68, Kurihara).

Arroyo et al. teach that the substituted check bits in each code word equal a set of bits in one of the unused syndromes (col. 10, lines 31-33, Arroyo et al.).

- As per claim 23, Kurihara, Fielder et al. and Arroyo et al. teach the additional limitations.

Arroyo et al. teach that the same logical value is a logical 1, and wherein each bit in the substituted check bits in each code word equal s an inverse logical value of each bit in one of the unused syndromes (col. 9, line 50-col. 10, line 3, Arroyo et al.).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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